

an addressing circuit which enables the combined subpixel outputs stored on said pixel's intrinsic capacitance to be read out in response to an address input.

REMARKS

This amendment is in response to the Office Action dated 7/19/02. As noted above, the present amendment is made in accordance with 37 C.F.R. § 1.116. Entry of this Amendment and reconsideration of this application are respectfully requested.

Claim Rejections under §103

Claims 8 and 12-14 were rejected as obvious over a patent to Takahashi. In response, claims 8 and 12 have been canceled. Claim 13 has been amended to depend from an allowable claim (claim 15), and claim 14 is allowable due to its dependence on claim 13.


Rewritten in Independent Form

Per the Examiner's suggestion, claims 9 and 15 have been rewritten in independent form. Claim 9 was rewritten to incorporate the limitations of its parent claim 8, and claim 15 was rewritten to incorporate the limitations of its parent claim 12; there were no intervening claims.

Claim 13 was amended to depend from the rewritten claim 15, and should thus be allowable. Claim 14 depends from claim 13, and thus should also be allowable as is.

All of the claims presently in the application are believed to be in proper form for allowance. A Notice of Allowance is respectfully requested.

Respectfully submitted,



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Attachment A:

Amended claims with insertions and deletions indicated.

9. (amended) A photodetector array with selectable resolution, comprising: [The photodetector array of claim 8, wherein]
a plurality of photodetectors;
a switching circuit which configures neighboring ones of said photodetectors into pixels by directly summing at each pixel the outputs of multiple photodetectors into an aggregated pixel output, said aggregated pixel output stored on said pixel's intrinsic capacitance prior to being read out;
wherein said switching circuit is electronically switchable to aggregate said photodetector signals according to at least two different selectable pixellization schemes with differing resolutions, such that said switching circuit combines photodetector signals according to at least two different, electronically selectable configurations: a first configuration in which each pixel output is a sum of two neighboring photodiodes; and a second configuration in which each pixel output is a sum of at least three photodiodes; and
a plurality of addressable interface circuits, each of which enables the aggregated pixel output stored on a respective one of said pixel's to be read out in response to an address input.

13. (amended) The photodetector array of claim 15[12], wherein said array is switchable between 1920 rows and 1080 rows.

15. (amended) A photodetector array, comprising a plurality of pixels, [The photodetector array of claim 12, wherein] said array of pixels [comprises] comprising a plurality of pixels arranged into at least three horizontal rows and vertical col-

umns,

wherein each pixel comprises an association of at least two subpixels;

and wherein the outputs of said subpixels are switchably combined into at least two different grouping arrangements, to give at least two different selectable pixel configurations, wherein said at least two different grouping arrangements comprises two different grouping arrangements, one of which combines the outputs of two adjacent subpixels in a given vertical column, and the other of which combines the outputs of three adjacent subpixels in said given vertical column,

each of said pixels having an intrinsic capacitance which stores said combined subpixel outputs prior to their being read out, and

an addressing circuit which enables the combined subpixel outputs stored on said pixel's intrinsic capacitance to be read out in response to an address input.